Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Previously presented) A rate matching circuit for adjusting the number of bits in a data block, the data block comprising a plurality of interleaved words generated by the action of an interleaving circuit on a coded output generated by the action of a coding circuit on a digital input, the coded output having a greater number of bits than the digital input, the rate matching circuit having means for adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, and means for selecting the rate matching pattern depending on an associated bit deletion or repetition pattern that is selected to ensure that deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed.

2. (Canceled)

3. (Previously presented) A rate matching circuit as claimed in claim 1, wherein the rate matching pattern for each interleaved word within the data block is offset with respect to the rate matching pattern of an adjacent interleaved word or words within the block.

4. (Previously presented) A rate matching circuit as claimed in claim 1, wherein the rate matching pattern is selected as a function of an interleaving depth of the interleaving circuit.

Claims 5-9. (Cancelled)

10. (Previously presented) A method of operating a rate matching circuit to adjust the number of bits in a data block, the data block comprising a plurality of interleaved words generated by the action of an interleaving circuit on a coded output generated by the action of a coding circuit on a digital input, the coded output having a greater number of bits than the digital input, the rate matching circuit adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, and selecting the rate matching pattern depending on an associated deletion or repetition pattern that is selected to ensure that deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed.

11. (Currently amended) The rate matching circuit of claim 1, wherein the rate matching pattern forms a matrix including change bits that indicate a change of corresponding bits of a matrix of said interleaved words within said data block, wherein each row of said matrix formed by the rate matching pattern includes a maximum of one of said change bits.

12. (Previously presented) The rate matching circuit of claim 1, wherein said coding circuit has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source.

13. (Previously presented) The rate matching circuit of claim 1, wherein said interleaving circuit is not adaptive.

14. (Previously presented) The rate matching circuit of claim 1, wherein said interleaving circuit has a constant input bit rate.

15. (Previously presented) The rate matching circuit of claim 1, wherein said coding circuit has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source, and wherein said interleaving circuit

16. (Previously presented) The rate matching circuit of claim 1, wherein said rate matching circuit alters a coding rate of said coding circuit according to the bit deletion or repetition pattern.

17. (Previously presented) The method of claim 10, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and the change bits are offset with respect to each other.

18. (Previously presented) The method of claim 10, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and the change bits are offset with respect to each other along adjacent columns of a matrix of said rate matching pattern.

19. (Previously presented) The method of claim 10, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent rows of a matrix of said rate matching pattern.

20. (Previously presented) The method of claim 10, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent rows and columns of a matrix of said rate matching pattern.

21. (Previously presented) The method of claim 10, wherein said interleaving circuit forms said data block by filling a matrix row by row with row bits of said coded output and outputting column bits of said matrix column by column to form said interleaved words.